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Product Specification

IEEE 802.11 a/b/g/n 2.4GHz 1T1R WiFi Module

Project Name	**QCA4004 11 b/g/n WIFI Module**	
Model NO	**FN-4004 (External antenna)**	
Customer		
Customer's Part NO		
Drafted: SJ LI	Approved: SYMEN	Sales: Sunny LIU

Feedback of customer's Confirmation

We accept the specification after Confirmed.

Customer	**Customer signature**	**Approved Date**

CONTENTS

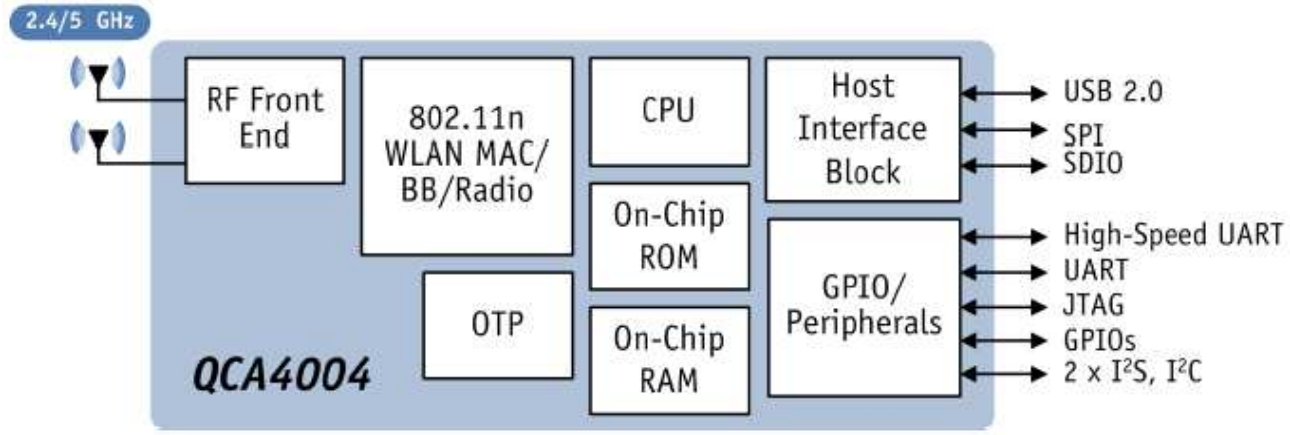
0. Revision History

REV NO	Date	Modifications	Draft
Rev0.1	2014-6-26	First Released	SJ LI

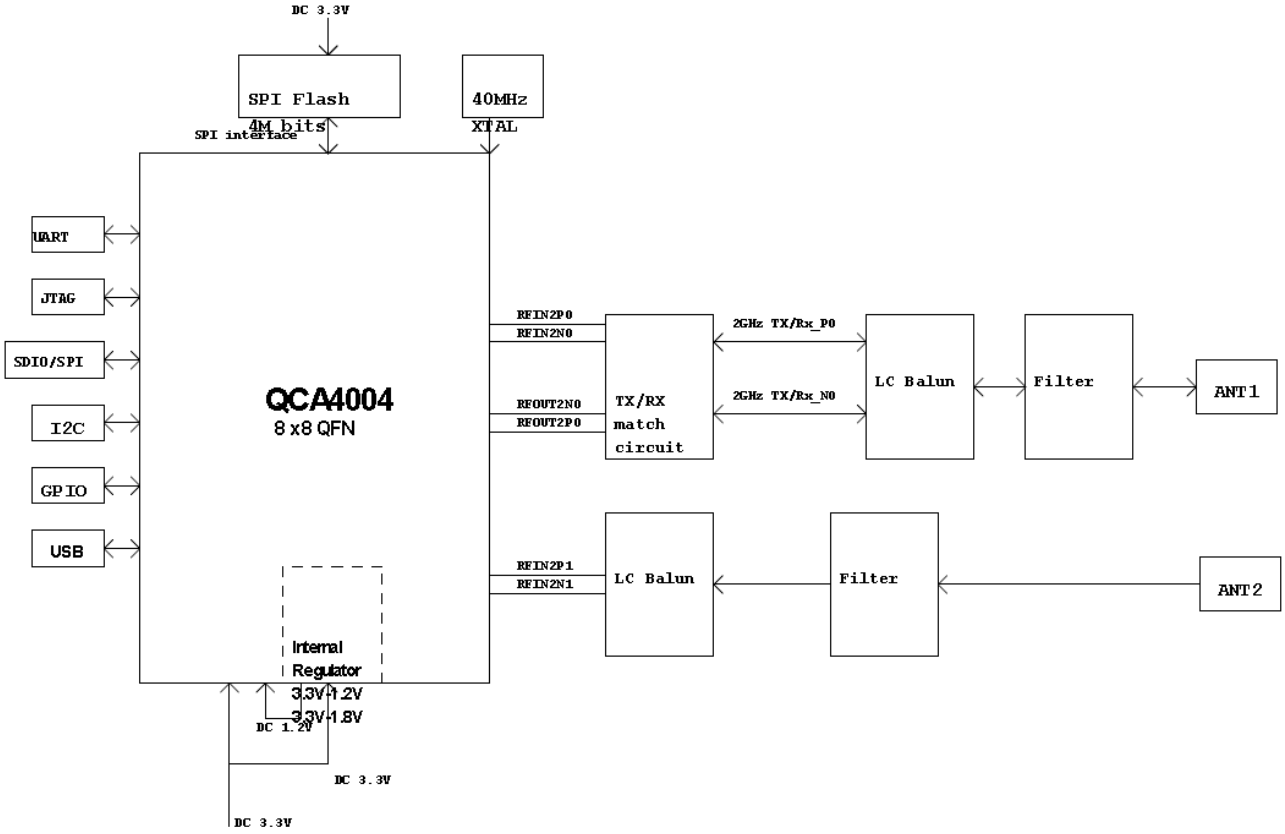
1. Introduction

1.1 Overview

The QCA4004 is a single chip 1x1 802.11b/g/n MIMO solution optimized for low-power embedded applications with single-stream capability for both transmit and receive. Frame aggregation, reduced inter-frame spacing (RIFS), and half guard intervals provide improved throughput on the link. Additional 802.11n performance optimization, such as 802.11n frame aggregation (A-MPDU and A-MSDU), is provided by drivers that support SDIO bus transaction bundling (a form of bus aggregation) and low-overhead host assisted buffering (Rx A-MSDU and A-MPDU). These techniques can improve the performance and efficiency of applications involving large bulk data transfers (for example, file transfers or high-resolution video streaming). The typical data path consists of the host interface, mailbox DMA, AHB, memory controller, MAC, BB, and radio. The CPU drives the control path via register and memory access. External interfaces include USB LPM or SPI slave, reference clock, and front-end components, as well as optional connections such as UART, SPI/I2C, GPIO, JTAG. See the "System Block Diagram"



1.2 Product Block Diagram



1.3 Product Features

- ◆ All-CMOS IEEE 802.11b/g/n 1x1 single-chip
- ◆ Support TCP/UDP IP protocol
- ◆ Support Smartconfig
- ◆ USB 2.0 at 480 Mbps using an integrated controller and PHY
- ◆ Extensive hardware support for WLAN coexistence through LPC message passing
- ◆ Power and clock management for extended battery life
- ◆ Green-Tx power saving
- ◆ Low-power listen mode and radio retention for reduced receive power consumption and sleep current
- ◆ Support for transmit beam formee (TxBFee)
- ◆ Integrated PA, LNA minimizing external component count
- ◆ Optional external PA, LNA support
- ◆ Data rates of up to 54 Mbps for 802.11g and 72.2 for 802.11n HT20, 150 Mbps for HT40
- ◆ Advanced power management to minimize standby, sleep and active power
- ◆ Security support for WPS, WPA2, WPA, WAP and protected management frames
- ◆ Block ACK
- ◆ GPIO/PWM/UART for console support
- ◆ JTAG-based processor debugging supported

2. GENERAL SPECIFICATION

2.1 WiFi RF Specifications

Features	Descriptions
Main Chipset	QCA4004
Frequency Range	2.400～2.484GHz
Operating Voltage	3.3Vdc ±10% supply voltage
Host Interface	**WiFi:** UART / SPI
Standards	**WiFi:** IEEE 802.11b, IEEE 802.11g, IEEE 802.11n,
Modulation	**WiFi:** 802.11b: CCK(11, 5.5Mbps), QPSK(2Mbps), BPSK(1Mbps), 802.11 g/n: OFDM
PHY Data rates	**WiFi:** 802.11b: 11,5.5,2,1 Mbps 802.11g: 54,48,36,24,18,12,9,6 Mbps 802.11n: up to 150Mbps
Transmit Output Power	**WiFi:** 802.11b@ 1Mbps 15**±2**dBm 802.11b@11Mbps 15**±2**dBm 802.11g@6Mbps 15**±2**dBm 802.11g@54Mbps 13**±2**dBm 802.11n@65Mbps 15**±2**dBm (MCS 0_HT20) 13**±2**dBm (MCS 7_HT20) 15**±2**dBm (MCS 0_HT40) 13**±2**dBm (MCS 7_HT40)
EVM	802.11b /11Mbps : EVM≦-9dB 802.11g /54Mbps : EVM≦-27dB 802.11n /MCS 7 : EVM≦-28dB
Receiver Sensitivity (HT 20)	**802.11b@8% PER** 1Mbps -90±1dBm 2Mbps -88±1dBm 5.5Mbps -86±1dBm 11Mbps -84±1dBm
	802.11g@10% PER 6Mbps -86±1dBm 9Mbps -85±1dBm 12Mbps -84±1dBm

	18Mbps -82±1dBm 24Mbps -80±1dBm 36Mbps -77±1dBm 48Mbps -73±1dBm 54Mbps -71±1dBm
	802.11n@10% PER MCS 0 -83±1dBm MCS 1 -82±1dBm MCS 2 -80±1dBm MCS 3 -78±1dBm MCS 4 -75±1dBm MCS 5 -71±1dBm MCS 6 -69±1dBm MCS 7 -67±1dBm
Operating Channel	**WiFi 2.4GHz:** 11: (Ch. 1-11) – United States(North America) 13: (Ch. 1-13) – Europe 14: (Ch. 1-14) – Japan
Media Access Control	**WiFi:** CSMA/CA with ACK
Network Architecture	**WiFi:** Ad-hoc mode (Peer-to-Peer) Infrastructure mode Software AP WiFi Direct
Security	**WiFi:** WPS, WPA2, WPA, WAP
Antenna	External antenna
Dimension	Typical L25.0*W18.0*T2.2mm

2.2 Sleep State Management

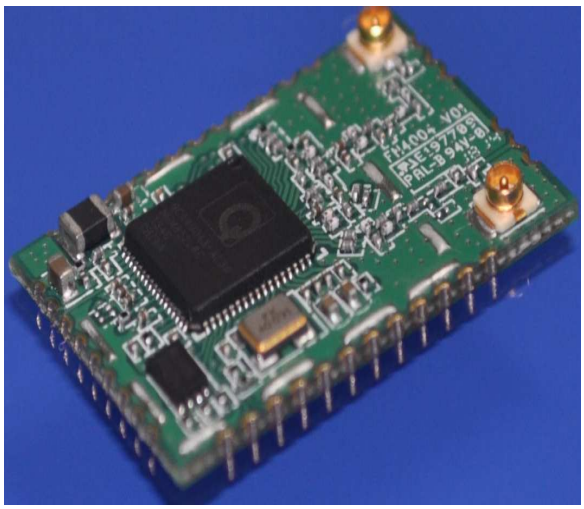
State	Descriptions
OFF	CHIP_PWD_L pin assertion immediately brings the chip to this state.
	Sleep clock is disabled.
	No state is preserved.
SLEEP	Only the sleep clock is operating.
	The crystal or oscillator is disabled.
	Any wakeup events (MAC, host, LF timer, GPIO interrupt) force a transition to WAKEUP.
	All internal states are maintained.
WAKEUP	The system transitions from sleep/OFF states to ON.
	The high frequency clock is gated off as the oscillator is brought up and the PLL is enabled.
	WAKEUP duration is usually 2 ms.
ON	The high speed clock is operational and sent to each block enabled by the clock control register.
	Lower-level clock gating is implemented at the block level, including the CPU, which can be gated off using WAITI instructions while the system is on. No CPU, host, or WLAN activities go to sleep.

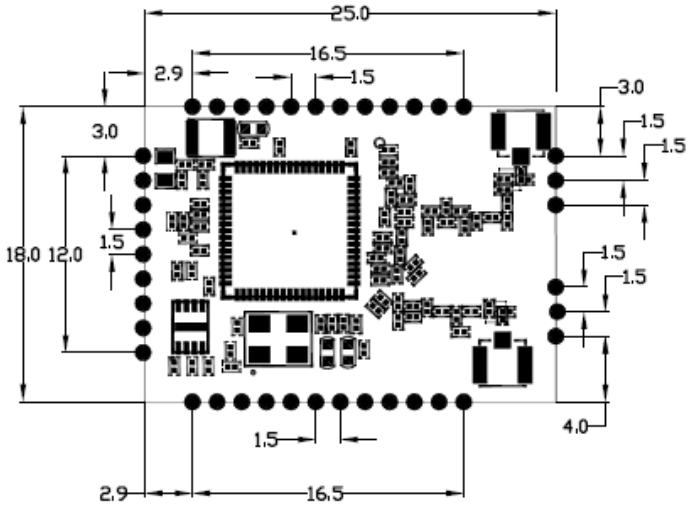
2.3 Power Consumption (unit: mA)

STATUS			Power Consumption
Power ON (Standby)			70
TX POWER	HT20	11n MCS0 TX	250
		11n MCS7 TX	220
		11g 6M TX	250
		11g 54M TX	230
		11b CCK1M TX	280
		11b CCK11M TX	275
	HT40	11n MCS0 TX	250
		11n MCS7 TX	220
RX POWER			105
SLEEP			7
DISABLE			7

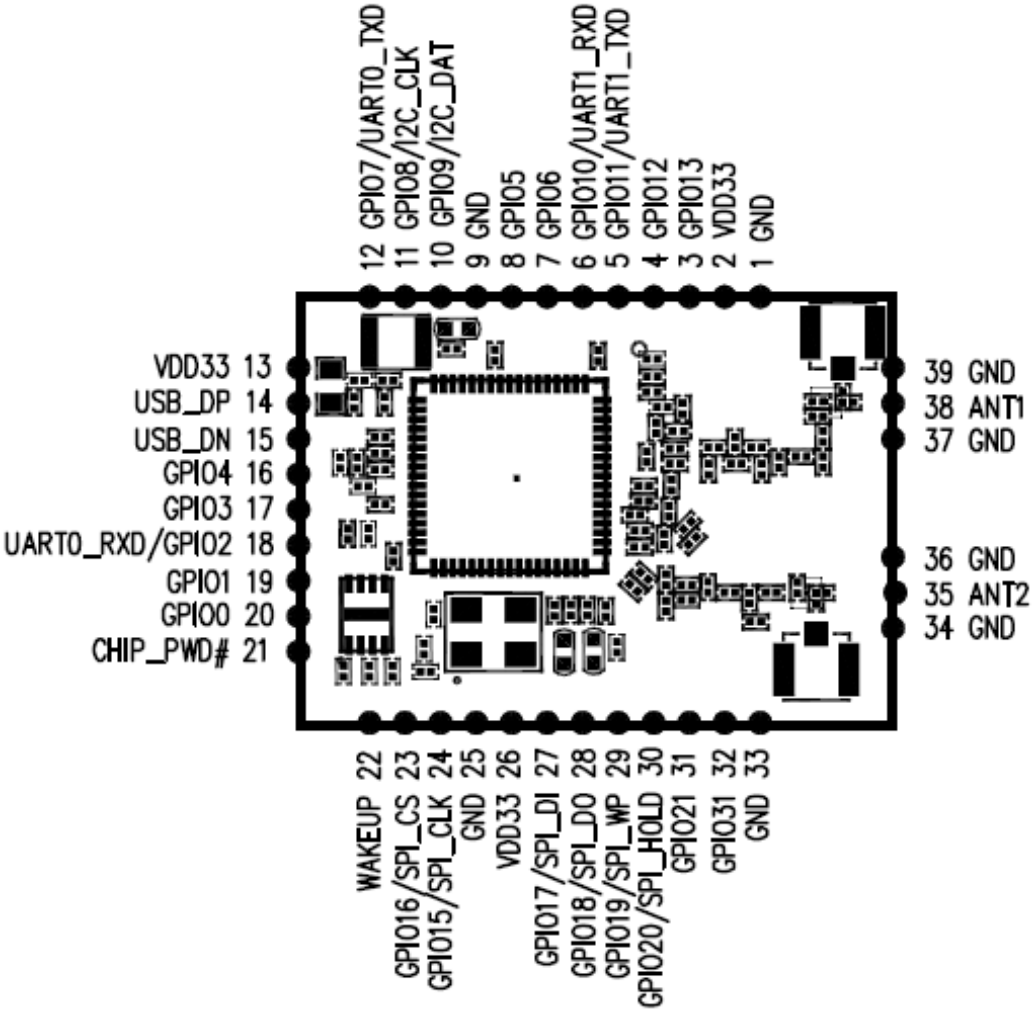
3. Mechanical Specification

3.1 Outline Drawing (Unit: ±0.15mm)





3.2 PIN Assignment



Pin #	Name	Description
1	GND	GROUND
2	VDDIO_HOST	3.3V Power
3	GPIO13	GPIO
4	GPIO12	GPIO

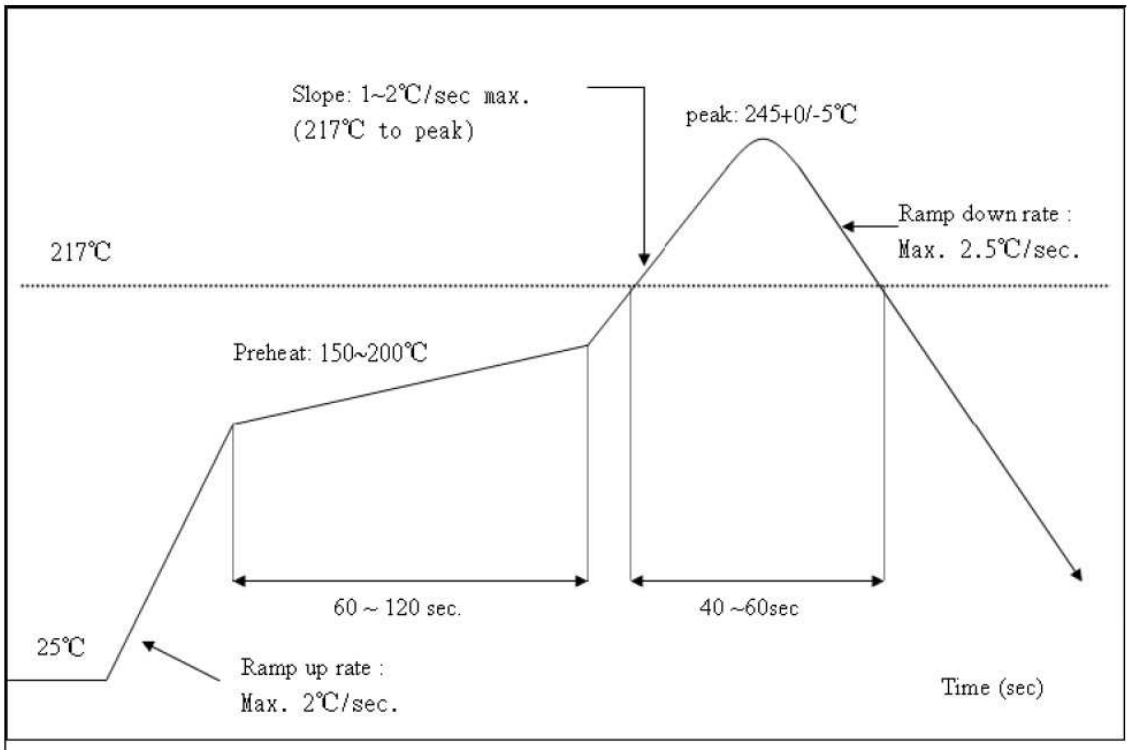
5	GPIO11/UART1_TXD	TXD1
6	GPIO10/UART1_RXD	UART1_RXD
7	GPIO6	GPIO
8	GPIO5	GPIO
9	GND	GROUND
10	GPIO9/I2C_SDA	I2C DATA
11	GPIO8/I2C_SCK	I2C CLOCK
12	GPIO7/UART0_TXD	TXD0
13	VDD33	3.3V Power
14	USB_DP	USB D+
15	USB_DN	USB D-
16	GPIO4	GPIO
17	GPIO3	GPIO
18	GPIO2/UART0_RXD	RXD
19	GPIO1	GPIO
20	GPIO0	GPIO
21	CHIP_PWD	CHIP ENABLE
22	WAKEUP	Wake-up
23	GPIO16/SPI_CS	SPI_CHIP SELECT
24	GPIO15/SPI_CLK	SPI_CLOCK
25	GND	GROUND
26	DVDD33	3.3V Power
27	GPIO17/SPI_DI	SPI_DATA INPUT
28	GPIO18/SPI_DO	SPI_DATA OUTPUT
29	GPIO19/SPI_WP	SPI_Write Protect
30	GPIO20/SPI_HOLD	SPI_HOLD
31	GPIO21/PWM_OUT	PWM_OUTPUT
32	GPIO31	GPIO
33	GND	GROUND
34,36	GND	RF Ground
35	EXT_ANT2	NC
37，39	GND	RF Ground
38	EXT_ANT1	External Antenna (2.4GHz 50Ohm)

4. Environmental Requirements

4.1 Operating& Storage Conditions

Operating	Temperature: 0°C to +55°C
	Relative Humidity: 10-90% (non-condensing)
Storage	Temperature: -40°C to +80°C (non-operating)
	Relative Humidity: 5-90% (non-condensing)

4.2 Recommended Reflow Profile
Referred to IPC/JEDEC standard.
Peak Temperature : <250°C
Number of Times : ≤2 times



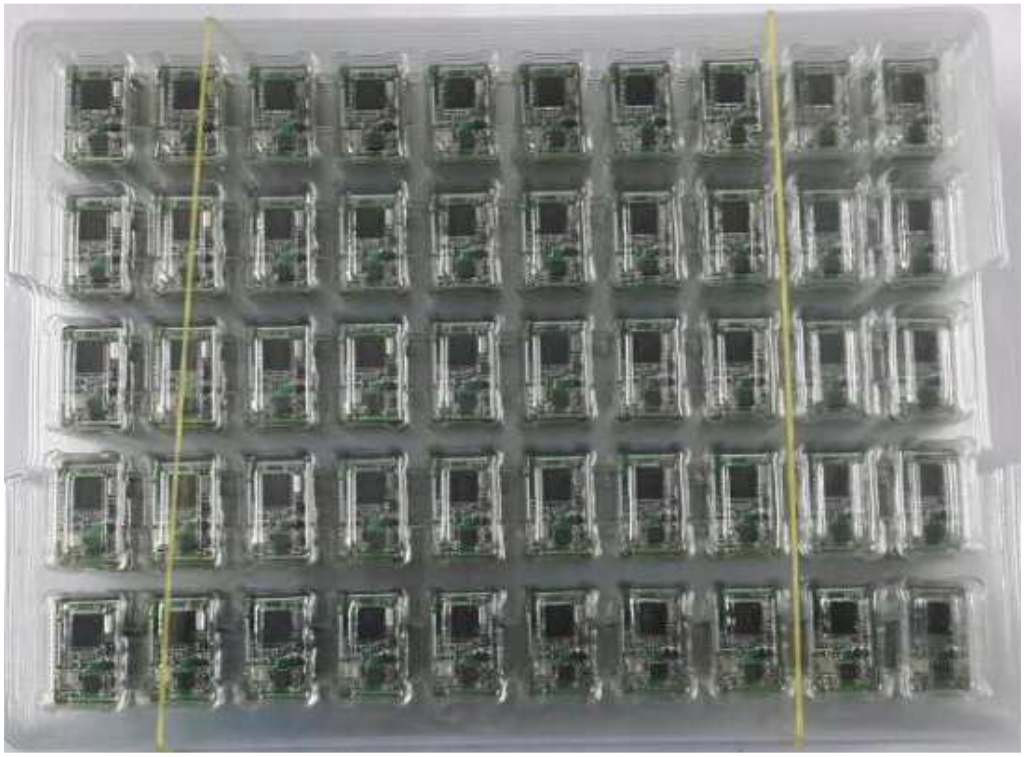
4.3 Patch WIFI modules installed before the notice:

WIFI module installed note:
1. Please press 1 : 1 and then expand outward proportion to 0.7 mm, 0.12 mm thickness When open a stencil
2. Take and use the WIFI module, please insure the electrostatic protective measures.
3. Reflow soldering temperature should be according to the customer the main size of the products, such as the temperature set at 250 + 5 ℃ for the MID motherboard.

About the module packaging, storage and use of matters needing attention are as follows:
1. The module of the reel and storage life of vacuum packing: 1). Shelf life: 8 months, storage environment conditions: temperature in: < 40 ℃, relative humidity: < 90% r.h.
2. The module vacuum packing once opened, time limit of the assembly:
Card: 1) check the humidity display value should be less than 30% (in blue), such as: 30% ~ 40% (pink), or greater than 40% (red) the module have been moisture absorption.
2.) factory environmental temperature humidity control: ≦ 30% ℃, ≦ 60% r.h..
3). Once opened, the workshop the preservation of life for 168 hours.
3. Once opened, such as when not used up within 168 hours:
1). The module must be again to remove the module moisture absorption.
2). The baking temperature: 125 ℃, 8 hours.
3.) After baking, put the right amount of desiccant to seal packages.

5. PACKING INFORMATION

5.1 Blister packaging



Vacuum packaging

A piece of 50 PCS (500 pcs/bag)

THE END